HILEVEL Technology, Inc.

Q'n Apps #P18

Q: What should I know about prober fixtures?

One popular use of HILEVEL testers involves exercising the DUT while on a probe station, especially in Failure Analysis labs. Some dock directly using a manipulator, but for others prober cabling is a compelling attraction. Here are some important considerations:

Cables

The length and quality of your cabling is extremely important, especially at speeds above 1 or 2 MHz. Use of poor quality cables (ordinary ribbon or other unshielded cables with mismatched impedance) can make even the most expensive testers perform poorly. Use 50Ohm coax or a shielded ribbon cable at 50Ohms with ground lines between each signal line.

Excessive cable length can introduce problems that are difficult to find. Each foot of cable adds about one and one-half ns to the data path, both for the tester and the DUT. Be sure to allow for this in your timing assignments, and sometimes within your translation or simulation; if compares or other edges are near the end of the cycle, you may have enough ñturn-aroundò delay that vectors must be skewed so that the compares can be done early in the next cycle. Keep your cables as short as possible. In our illustration we show 3-foot cables, which should be considered a maximum length. This method is called ñsoft dockingò and is the lowest in cost, but the environment is not very ñcleanò at faster test rates. Hard docking (also called ñdirect dockingò) is the best for signal integrity, but tester fan vibration can be transferred to the prober and can be difficult to manage, and the manipulators are expensive. The most cost effective approach is something we call ñfirm dockingò. By using a low-cost manipulator and positioning the test head close to the probe site, very short cables and be used while isolating the prober from vibration.

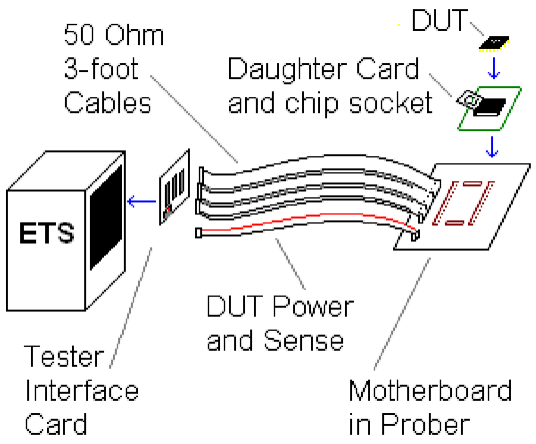
Daughter Card

Your cables will typically connect to some type of motherboard under the prober, which then receives various daughter cards (or probe cards) that route signals and power to different types of DUTs. We have seen the greatest successes in this type of arrangement when daughter cards and their interface is built in such a way that allows them to be connected to fixturing directly on the front of the tester as well as to the motherboard in the prober. This allows you to develop your tests without the hazards of remote cabling slowing you down, and also helps you to diagnose problems introduced by the prober fixturing if they should occur. When you move your daughter card to the prober you can see exactly how much effect your fixturing has on the performance of the DUT. Pay close attention to the spacing between signal connectors on the front of the tester and be aware of acreage displacement needed on your daughter card to fit between these connectors.

Power and Ground

We do not recommend bringing DUT power and ground to the prober by way of the same ribbon cables carrying signals, but rather to run separate leads for them. If you plan to do any Iddq measurements you must also bring up the sense lines; on the DUT board the sense is identified by "S+" and "S-" next to the DUT supply pads. Be sure to cut the etch joining the sense lines to Vdd plus and minus at the DUT board, and do not reconnect sense to power until "the last possible centimeter" of connection to the DUT. You will also need .01 and/or .1 uf bypass capacitors right at the power pins of the DUT chip socket for a local reservoir of power. Keep the leads as short as possible, and No Electrolytics!

See the illustration on the next page.



Typical Prober Interface

DUT Drive and Loading

Knowledge of your chip is a crucial tool for cable interface preparation. Devices with 20mA of drive current on output pins should have little trouble with a clean 50Ohm environment. If your DUT has very low drive capability it may have difficulty driving back to the tester and overcoming "line charge".

The phenomenon of line charging is a natural occurrence that can play a frustrating role in your test development. It becomes a factor on bidirectional data lines when the tester drives logic high for one or more vectors and then switches direction so that the DUT can drive data back to the tester. These data lines will have been "charged" by the system driving the desired logic level through the cables, and even though the tester drivers will have been tristated for the direction change, the cables can remain charged for quite some time - perhaps many microseconds - as the charge slowly drains off. If your chip or fixturing does not have sufficient loading to drain this charge, it will appear to the DUT that tester is still driving when your chip attempts to output data. On the scope, this may look like signal contention, and it makes good timing measurements impossible.

There are three recommended ways to attack this problem:

1. Avoid the transition area. This means that you must test with your compare strobes placed well past the "contention" period, and may force you to run very slow. Timing measurements are not very meaningful in this approach.

2. Load resistors at the DUT. This can be effective, but messy. Also you must consider whether or not your DUT can drive the cables after battling the load resistors. Typically a pull-up/pull-down arrangement using 1K to 10K resistors is applied, depending on the chip's tolerance to loads.

3. HiLevel programmable loads. Probably the easiest and cleanest cure, these loads allow you to program actual Ioh and Iol current potentials via software. These active loads are at the tester, so the DUT does not have to overcome loads before driving the cables. Again, you must consider the overall drive capability of your DUT.

Related info

Q'nApp #P1: The PinList Function
Q'nApp #P9: Iddq Testing
Q'nApp #P20: Power & Ground
Q'nApp #P22: Bypass Capacitors
Q'nApp #P34: DUT board compatibility
Q'nApp #P37: MultiSite
Q'nApp #P46: TDR Check
Q'nApp #P51: Fast Continuity
Q'nApp #P61: Pin-to-pn Resistance